Corrected Drawings, which includes a complete set of drawings (54 sheets, Figs. 1a-33) that incorporates the approved changes to Figs. 1a, 1b, 2a and 2b.

IN THE CLAIMS:

Applicants respectfully request that claims 2, 12 and 18 be amended to read as follows (a marked-up version of the claims appears in the attached Appendix):

2. A semiconductor memory device comprising:

a semiconductor substrate;

a plurality of trench capacitors formed in said semiconductor substrate and arranged at a regular pitch;

a semiconductor layer formed on said semiconductor substrate in which said trench capacitors are formed;

an element isolation insulating film buried in said semiconductor layer to define a plurality of active element areas each spreading over two adjacent trench capacitors;

a plurality of transistors formed two by two in each of said plurality of active element areas, such that two transistors share one of source/drain diffusion layers, and the other of said source/drain diffusion layers is positioned over trenches of two adjacent trench capacitors, said transistors each having a gate connected to a word line continuous in one direction;

a contact layer for connecting the other of said source/drain diffusion layers of each of said transistors to a capacitor node layer of corresponding one of said trench capacitors; and

a bit line provided to intersect said word lines and connected to one of said source/drain diffusion layers of said transistor.

12. A semiconductor device comprising:

a semiconductor substrate;

an element isolation insulating film including a first insulating film buried to define active element areas on said semiconductor substrate, and a second insulating film shallower and wider than said first insulating film and positioned over the first insulating film; and

B2

elements formed in said active element areas defined by said element isolation insulating film, said elements including a capacitor node formed in a trench in said semiconductor substrate, and a contact layer contacting an upper surface of said capacitor node, wherein said contact layer is formed in a contact hole in said semiconductor substrate.

B3

18. The device of claim 12, wherein said contact layer contacts an underside of second insulating film, and a side of the first insulating film.

REMARKS

Claims 2-12 and 18 were pending in the Action. Claims 2 and 6-10 stand rejected under 35 U.S.C. 102(b) as being anticipated by *Park et al.* (U.S. Patent No. 5,521,115). Claims 12 and 18 stand rejected under 35 U.S.C. 102(b) as being anticipated by *Ushiku et al.* (U.S. Patent No. 5,675,176). Claim 11 stands rejected under 35 U.S.C. 103(a) as being obvious over *Park et al.* in view of *Bronner et al.* (U.S. Pat. No. 5,606,188). Claims 3-5 stand rejected under 35 U.S.C. 103(a) as being obvious over *Park et al.* in view of *Ishii* (U.S. Pat. No. 5,250,831).